3.4V OPERATION 1W MMIC POWER AMPLIFIER WITH $SrTiO_3$ CAPACITORS FOR DIGITAL CELLULAR PHONES

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ABSTRACT

This paper describes 950MHz power performance of a two-stage MMIC amplifier utilizing n-AlGaAs/InGaAs/n-AlGaAs FETs and $SrTiO_3$ capacitors. Under 3.4V drain bias operation, the MMIC with 2.0×2.4mm^2 area delivered a π/4-shifted QPSK output signal of 0.8W (29.0dBm), a power-added efficiency (PAE) of 30% and an associated gain of 26.4dB with an adjacent channel leakage power at 50kHz off-center frequency of -50.5dBc. It also achieved a saturated output power of 1.1W with PAE of 39%.

INTRODUCTION

In recent wireless communication systems, small size and high efficiency MMIC power amplifiers are strongly demanded. Recently, GaAs MESFET MMIC power amplifiers for cellular phone applications have been reported. A GaAs MMIC power amplifier with 2.5×3.48mm^2 area exhibited a saturated output power of 1.1W for analogue cellular applications at a drain bias voltage (V_d) of 3.3V[1]. For CDMA/AMPS dual mode cellular applications, an MMIC power amplifier with 2.5×2.9mm^2 area delivered an output power (P_{out}) of 0.53W at V_d = 4.7V. However, 3.4V operation MMIC power amplifiers for digital cellular applications with 1W P_{out} have not been reported yet. In this work, a 2.0×2.4mm^2 sized 1W MMIC amplifier for 3.4V digital cellular phone applications has been successfully fabricated.

DESIGN AND FABRICATION

The fabricated MMIC power amplifier utilized n-AlGaAs/InGaAs/n-AlGaAs Hetero-junction FETs (HJFET) and $SrTiO_3$ (STO) capacitors.

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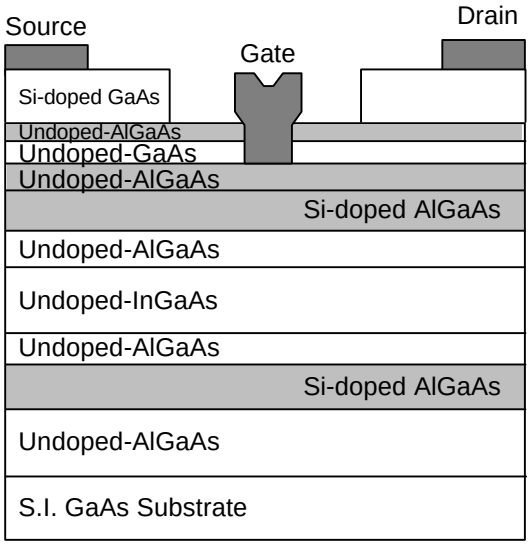

Figure 1 Cross section of the HJFET

Figure 1 shows the cross section of the fabricated HJFET. An undoped AlGaAs Schottky layer was incorporated on the upper Si-doped AlGaAs layer to achieve a sufficiently high breakdown voltage[3]. Furthermore, an undoped GaAs layer and an undoped AlGaAs layer were incorporated between the AlGaAs Schottky layer and an Si-doped GaAs cap layer, as etch stop layers. With this epitaxial wafer, a double recessed structure was fabricated by electron cyclotron resonance plasma dry-etching using SF_6 and BCl_3[3]. A 1.0μm long WSi Schottky gate was fabricated on the recessed AlGaAs Schottky layer. Figure 2 shows typical drain current (I_d) versus drain-to-source voltage (V_{ds}) characteristic for the fabricated HJFET. The HJFET exhibited a maximum I_d of 500mA/mm with a high gate-to-drain breakdown voltage of 20V. The threshold voltage was -0.8V with 20mV standard derivation on a 3 inch wafer.

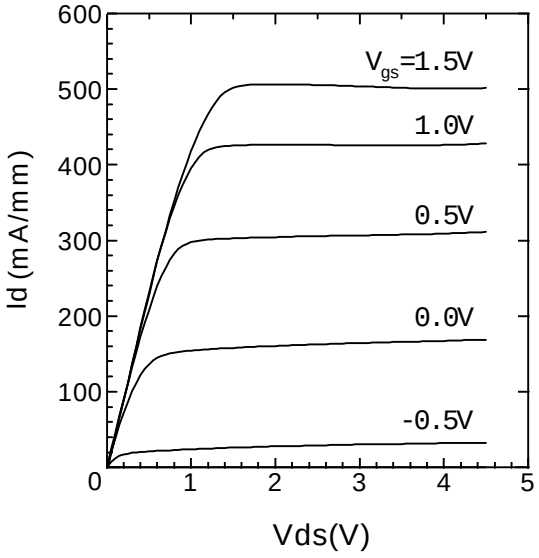

Figure 2 Drain I-V Characteristics of the HJFET

Figure 3 shows the cross section of the fabricated STO capacitor employed in the MMIC. The capacitor consists of a Pt/Ti/Pt/Ti stacked base electrode to achieve high tolerance under ion-milling of STO. This results in low electrode resistance[4]. A 200nm-thick STO film was deposited on the base electrode by an RF-sputtering method at a substrate temperature of 450°C. The capacitor exhibited a dielectric constant (ε_r) of 180. This high ε_r was reported to be constant up to 20GHz[4]. The breakdown voltage defined at a 10mA/cm^2 leakage current was 50V.

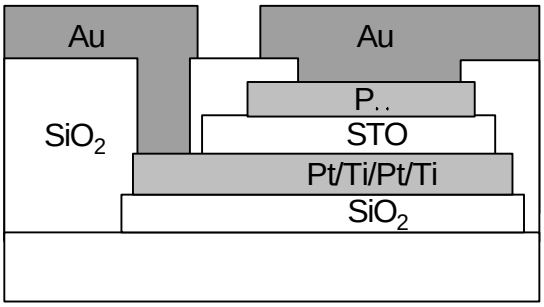

Figure 3 Cross section of the STO capacitor

The circuit configuration of the fabricated one-chip MMIC power amplifier is shown in Figure 4. The MMIC includes a two-stage HJFET amplifier with input and output matching circuits as well as bias circuits utilizing STO capacitors. Two FETs with W_g=3.5mm and 17.5mm were directly connected with a series capacitor. At 950MHz, the output impedance of the first-stage FET was 3.5+j5.5Ω, whereas the input impedance of the second-stage FET was 1.0+j2.5Ω. These rather similar matching impedances, which are due to the proper choice of the gate width, enable connection without a complicated matching circuit. The output matching circuit was designed for maximum output power. This also achieved minimized distortion characteristics. The drain bias circuit for the second-stage FET was designed to exhibit high impedance at the fundamental frequency. Spiral inductors with 100μm wide and 5μm thick plated Au were employed to reduce DC and RF loss.

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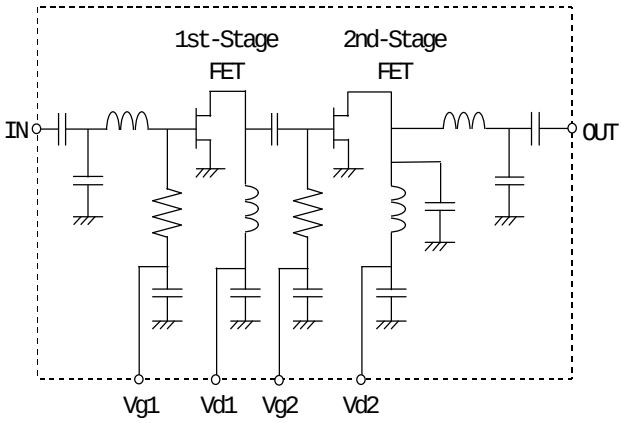

Figure 4 Schematic circuit of the MMIC

Figure 5 shows a photograph of the developed MMIC amplifier. The chip size is 2.0×2.4mm^2. High power density of the HJFET and high ε_r of the STO capacitor resulted in substantial reduction in the size of MMIC.

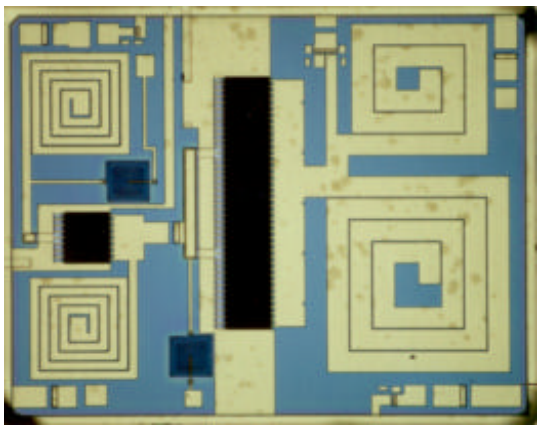

Figure 5 Photograph of the MMIC amplifier

RESULTS

For personal digital cellular (PDC) applications, 950MHz power performance of the MMIC power amplifier was evaluated at drain bias voltages (V_{d1},V_{d2}) of 3.4V, which corresponds to the DC operating voltage for PDC system when one Li-ion battery cell was used. The MMIC amplifier was operated at a gate bias voltage for the first-stage (V_{g1}) of -0.35V and those for the second-stage (V_{g2}) of -0.4V. Figure 6 shows small signal gain and output return loss as a function of frequency for the MMIC amplifier. The amplifier achieved small signal gain of 28.2dB with 1dB-gain-down bandwidth of 70MHz.

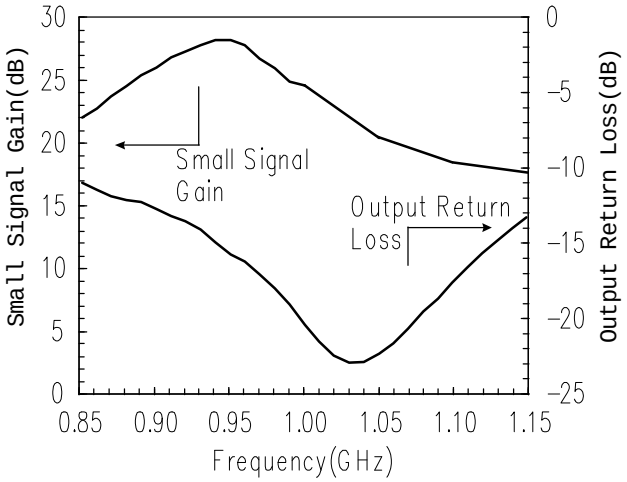

Figure 6 Small signal gain and output return loss versus frequency for the MMIC amplifier

Figure 7 shows P_{out}, power-added efficiency (PAE), adjacent channel leakage power at 50kHz off-center frequency (P_{adj}) and Gain as a function of input power (P_{in}) with a 950MHz $\pi/4$-shifted QPSK signal. The MMIC power amplifier exhibited P_{out} of 29.0dBm (0.8W), PAE of 30% and P_{adj} of -50.5dBc with associated Gain of 26.4dB. It also yielded a saturated output power of 30.5dBm (1.1W) and PAE of 39%. To the authors' knowledge, the fabricated MMIC is the first power amplifier satisfying the PDC criteria.

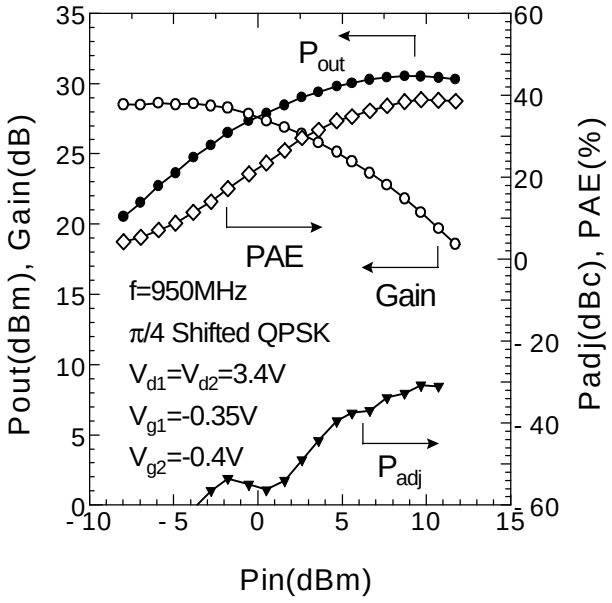

Figure 7 P_{out}, PAE, P_{adj} and Gain as a function of P_{in} for the MMIC amplifier

SUMMARY

We have developed a two-stage MMIC power amplifier with 2.0×2.4mm^2 area utilizing HJFETs and STO capacitors. For 950MHz PDC application, the amplifier exhibited P_{out} of 29.0dBm (0.8W), PAE of 30% and Gain of 26.4dB with P_{adj} of -50.5dBc under 3.4V drain bias operation. The developed MMIC power amplifier is promising for small and light weight digital cellular phones.

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